IN THE CLAIMS:

Claim 34 and 36 have been cancelled. Claims 30, 35, and 37 have been amended, as follows:

Claims 1 – 29 (cancelled)

30. (currently amended) A memory component comprising:

a random access memory array having a plurality of storage locations;

a timing input for receiving a timing signal which when [[activ]] active toggles between first and second states at a periodic rate; and

circuitry, coupled to the timing input and to the random access memory array, for transferring data to the memory component in synchronism with the timing signal and for transferring the data to the random access memory array.

31. (previously presented) The memory component of claim 30, wherein the random access memory array is a dynamic random access memory array.

32. (previously presented) The memory component of claim 30, wherein said circuitry includes a shift register.

33. (previously presented) The memory component of claim 30, wherein said circuitry includes a multiplexer.

Claim 34 (cancelled).

35. (currently amended) The memory component of claim [[34]] 37, wherein the random access memory array is a dynamic random access memory array.

Claim 36 (cancelled).

37. (currently amended) ~~The memory component of claim 34~~ A memory component comprising:

a random access memory array having a plurality of storage locations;

a timing input for receiving a timing signal which when active toggles between first and second states at a periodic rate; and

circuitry, coupled to the timing input and to the random access memory array, for receiving data from the random access memory array and for transferring the data from the memory component in synchronism with the timing signal, wherein said circuitry includes a multiplexer.